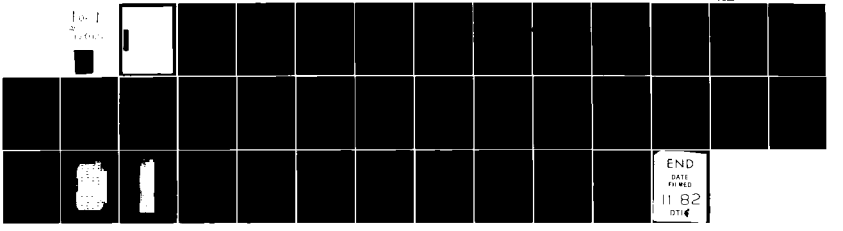
AD-A120 131 NAVAL RESEARCH LAB WASHINGTON DC F/G 17/2.1
WIDEBAND HF CHANNEL PROBER TIMING AND CONTROL MODULES.(U)
SEP 82 L S WAGNER, J A GOLDSTEIN
UNCLASSIFIED NRL-MR-4933 NL



SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: NRL Memorandum Report 4933	2. GOVT ACCESSION NO.: A120 131 / 3. RECIPIENT'S CATALOG NUMBER:
4. TITLE (and Subtitle): WIDEBAND HF CHANNEL PROBER — TIMING AND CONTROL MODULES	5. TYPE OF REPORT & PERIOD COVERED: Interim report on a continuing NRL problem. (6/78—7/82)
	6. PERFORMING ORG. REPORT NUMBER:
7. AUTHOR(s): L.S. Wagner and J.A. Goldstein	8. CONTRACT OR GRANT NUMBER(s):
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Naval Research Laboratory, Washington, DC 20375	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: RR021-05-42; 75-0141-0-2
11. CONTROLLING OFFICE NAME AND ADDRESS:	12. REPORT DATE: September 29, 1982
	13. NUMBER OF PAGES: 36
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office):	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Wideband communication	Pulse sounder	Timing circuits
Propagation	Microprocessor	HF Channel sounder
Pulsed systems	TTL Logic circuits	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The timing and control functions for the Wideband HF Channel Prober system have been implemented utilizing digital logic circuits and a microprocessor in a hybrid hardware - software design. The system's speed and flexibility requirement dictated which functions could and should be implemented in a microprocessor. Functions that required higher speed and less flexibility were implemented using TTL logic circuits. This report

(Continues)

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

20. ABSTRACT (Continued)

discusses the design criteria and the logic hardware and microprocessor software for implementing the design requirements of the timing and control functions of the Wideband HF Channel Prober apparatus.

CONTENTS

WIDEBAND HF CHANNEL PROBER — TIMING AND CONTROL MODULES

I. INTRODUCTION

The Wideband HF Channel Prober project is an experimental investigation of the HF (2 to 30 MHz) extended line-of-sight (ELOS) communication channel. Characterization of the channel for a bandwidth of 1 MHz is the major objective of the Channel Prober project. Because data collection must take place in real time, many system operations must be implemented in digital logic hardware. The logical functions are divided into two categories according to speed. The fastest functional operations take place in the Timing Module. The Control Module operations require flexibility and are less dependent upon speed. The Timing Module is implemented by standard TTL logic elements and the Control Module by a microprocessor. This report will discuss the design considerations and the resulting implementation of the Timing and Control Modules associated with the Wideband HF Channel Prober.

Details of other system components can be found in a separate formal report entitled "Wideband HF Channel Prober - System Description" (NRL Report 8622, in progress). In addition, the system computer real-time software is discussed in a separate NRL Memorandum report (in progress).

II. DESIGN OVERVIEW

A. Design Considerations

The Channel Prober experimental measurements involve two separated field sites, a transmitter site and receiver site, each acting in close coordination with the other. Coordination is accomplished by maintaining accurate time and frequency stability at both sites. The required frequency stability is derived from a rubidium frequency standard. Timing accuracy is established through the use of the rubidium frequency standard as a reference oscillator and by setting time according to the time standard information broadcast by WWV.

Early in the design phase a determination had to be made concerning the implementation of the timing and control functions. Two obvious candidates were a hard-wired logic device and a microprocessor. The hard-wired logic offered the advantage of high speed while the microprocessor offered the advantage of flexibility inherent in software design. The design that was chosen employs a hybrid system in which those functions that require high speed are implemented by hard-wired logic (The Timing Module), while the lower speed functions are implemented using a microprocessor (The Control Module).

In addition to satisfying system speed requirements and to providing the necessary flexibility for an experimental instrument, the choice of a hybrid design also resulted in an economy of parts. An example of this was provided in the early stages of system development when it was determined that frequency stepping could not simply be sequential but might have to allow skipping certain frequencies. A hard-wired logic design to implement a simple skip procedure was found to require a 200% increase in the number

Manuscript submitted September 10, 1982.

of integrated circuits. The use of a microprocessor (μP), with operating frequencies stored in a Random Access Memory (RAM) buffer, permitted almost unlimited flexibility without incurring additional hardware costs.

A small minicomputer (e.g. a Digital Equipment Corp. (DEC) Model PDP 11/05) was considered as an alternative to the μP. The minicomputer offers the advantage of more powerful software support and other "computing power" advantages. This approach was rejected because it entailed a cost premium for "computing power" not utilized by the control tasks. Other factors influencing the decision were the lower cost of μP replacement boards, the ease of on-site service to the μP by NRL personnel, and the higher reliability of the simpler, more compact, and lighter μP equipment.

The Timing Module generates the modulation signals used by the Channel Prober Exciter. The basic signal structural element is the pseudo-noise (PN) sequence. Two different PN sequences are used, one for the Prober mode and one for the Sounder mode. The Prober mode sequence consists of 2047 pulses (chips) while the Sounder mode sequence consists of 255 pulses (chips). The sequence period is approximately 8 msec in both modes and corresponds to a chip rate of 250 kHz in the Prober mode and 31.25 kHz in the Sounder mode.

The Timing Module also generates the pulse modulation for the Transmitter Exciter, a coherent 8 MHz clock required by the Correlation Processor, and the PN generator reference pulses for interrupting the μP at the end of each PN sequence. These pulses are the basic timing strobes of the "control" process. Speed requirements necessitated the use of hard-wire digital logic for these functions.

The Control Module (μP) treats the PN sequence reference pulses as system interrupts. A software interrupt routine counts the number of interrupts and switches frequency and operating mode depending on the number of completed PN sequences. The Control Module then distributes the various control signals to other system components for operation according to the prescribed format. Signals distributed to the Transmitter Exciter are the BCD encoded frequency information for the synthesizer that functions as the Exciter's second local oscillator and the mode flag for bandwidth switching. Signals distributed to the Receiver include the BCD encoded frequency information for the Receiver first local oscillator, BCD encoded signals for pre-selector control and the mode flag for bandwidth switching. In addition, the signals provided by the Control Module to the system Real-Time Processor, at the Receiver site, include the AGC sampling strobe, the frequency index number, the first and second sequence flags of a correlation cycle and the end of experiment flag.

B. Functional Description

A block diagram illustrating the "control" interaction of the major system modules is shown in Figure 1. The fundamental input to the Timing Module (TM) is the 1 MHz reference frequency from the Station Frequency

Standard. This input is controlled by the manual "clock on/off" switch, S1. Closure of S1 activates the Prober mode and Sounder mode clock circuits. Further action must await a "clock-start" gate which can be initiated automatically by the digital clock comparator circuit or manually by the "manual-start" switch, S2. Activation of "clock-start" forces a synchronization of the PN sequences, causes the PSK and pulse modulation signals to be gated to the Transmitter Exciter and gates the PN sequence interrupts to the μP. The arrival of interrupts at the Control Module signals the start of the prescribed experimental procedure. After the prescribed experimental procedure is completed, the μP sets a STOP flag which is distributed to the Timing Module and the DEC Model PDP-11/34 Real-Time Processor. Receipt of the STOP flag signal causes the Timing Module to revert to a "pre-start" condition, informs the PDP-11/34 of experiment termination and restores the μP software to a condition where it awaits the start of the next experiment.

The Control Module accepts interrupts from both the Sounder and Prober PN generators but, depending on the operating mode, only one of the interrupts is enabled. Upon detection of an interrupt, the μP increments the sequence count and executes the logic required to support the operational format. These operations are performed in a user-defined software interrupt handler routine.

Control variables generated by the Control Module include BCD signals for remote control of Transmitter and Receiver local oscillator frequencies and for the control of the Receiver pre-selector filter. In addition, a MODE flag for controlling the operational mode of the experiment, sequence flags for synchronizing the Correlation Processor with the action of the Transmitter, a Receiver AGC-voltage sampling strobe and a STOP flag signaling the end of a prescribed experimental procedure are also generated and distributed. As shown in Figure 1, the MODE flag is passed to the Timing Module to control its mode of operation. A complete PN sequence period, the "idle sequence", is allotted to the execution of these tasks; thus providing ample time for μP control.

Communication from the Control Module to the PDP-11/34 Real-Time Processor is implemented by a DEC Model DR 11C parallel interface board. Information passed includes the MODE flag, the STOP flag, the frequency pointer and sequence synchronizing flags. The sequence synchronizing flags are used by the Real-Time Processor to control the action of the Correlation Processor while the other variables are required for the proper identification and labeling of incoming data. Communication from the PDP-11/34 to the μP includes all operational details of the experiment about to be run. Once this information is passed, there is no further communication from the PDP-11/34 to the microprocessor until the experiment is complete and another experiment is to be run.

The next two sections of this report discuss details of the operation of the Timing Module (Section III) and the Control Module (Section IV).

III. Timing Module

Specific tasks assigned to the Timing Module are:

- o START/STOP control of the experiment clock
- o Generation of Sounder & Prober mode clock signals
- o Generation of the Sounder & Prober mode PN sequences and associated μP interrupts
- o Generation of an 8 MHz Correlation Processor clock

A functional block diagram of the Timing Module is present in Figure 2. All clock signals are derived from an ultra-stable Station Standard (rubidium frequency source) which also drives the Station Time Source. The Time Source is a digital time code generator and provides a BCD encoded output which is used in conjunction with a BCD comparator for the generation of the experiment "clock start" signal. More detailed circuit diagrams of the timing module are shown in Figures 3, 4, 5, 6 and 7.

The major components of the Timing Module are as follows:

- o ON/OFF and START/STOP circuits (Figure 3a)
- o Two-Phase Clock circuit (Figure 3b)
- o Sounder Mode PN Generator (Figure 4)
- o Prober Mode PN Generator (Figure 5)
- o Mode Condition Generator (Figure 6)
- o 8 MHz Phase Locked Loop (Figure 8).

The form of component interconnection is shown in Figure 2. Each of these subsystems is discussed separately in the ensuing sections.

A. ON/OFF and START/STOP Circuits

Circuits associated with the ON/OFF and START/STOP functions include those modules within the dashed lines of Figure 3a. These include switches S1 and S2, parts of TTL modules U1, U2, U3, U4, U21, U22, U39 and U40. The ON/OFF portion of the circuit is activated by setting S1 ON and results in a HIGH* at U21-10. The START/STOP circuit action is described by first noting that START is initiated either by the action of the BCD digital time comparator or by manual operation of switch S2 and results in the activation of line U3-5 (HIGH) at the first positive transition of U2-8. Thereafter, U3-5 remains HIGH until U3-1 is brought LOW following a STOP flag HIGH at U22-1.

---

*True logic is used for all circuits. Therefore HIGH is a logical "1" and LOW is a logical "0".

U3-5 HIGH is the system START flag. Events connected with U3-5 going HIGH are U3-9 LOW, which lights the RUN indicator, and a negative pulse out of U40-3, which initializes the Mode Condition Generator to the Sounder mode. In addition, U3-5 HIGH is responsible for gating the PN sequence to the Exciter PSK modulator (Figure 4), the clock signal to the Exciter pulse modulator (Figure 6) and the PN generator reference interrupts to the μP (Figures 4 and 5).

B. Two-Phase Clock Circuit

The Two-Phase Clock circuit is aways operating, as long as the 1 MHz reference signal is present. The Clock circuit generates two two-phase clock pulses at rates of 250 kHz and 31.25 kHz for use in the Prober and Sounder modes, respectively. The Clock circuit consists of elements of TTL modules U1, U5, U6, U7 and U8 and transistor Q1 in association with diode D1 and these modules are shown within the dashed lines of Figure 3b. The 1 MHz reference is converted to a square wave by the action of Q1 and D1. The 1 MHz square wave signal at U5-2 is the fundamental clock input to a counter-divider circuit consisting of U5 and U6. The divide by 2 and by 4 outputs (U5-14 and U5-13) are combined to generate the 250 kHz two-phase clock. The divide by 8 output of U5 (U5-12) drives the second counter (U6) at a 125 kHz rate, and the divide by 2 and by 4 outputs of U6 (U6-14, U6-13) are combined to generate the 31.25 kHz two-phase clock. The 250 kHz clock phase 1 signal drives a single-shot multivibrator U1-10 whose output U1-5 drives the "CLOCK-ON" indicator lamp.

The phase 1 clock signals are connected directly to the clock inputs of the PN generator shift registers (Figures 4 and 5). The phase 2 clock signal is gated to the Exciter pulse modulator (Figure 6) after activation of the system START flag. The appropriate clock, Sounder or Prober, is selected according to the MODE flag provided by the μP Control Module through the Mode Condition Generator (Figure 6).

C. PN Sequence Generator

The PN sequence generators produce the phase shift (BPSK) modulation signals used by the Channel Prober instrument. In addition, each generator circuit produces, for each sequence, a synchronizing pulse that is transmitted to the Control Module and serves as a μP interrupt signal. The signals and conditions required for proper PN Generator operation are:

- ON/OFF switch ON (U21-10 HIGH)
- START/STOP signal on START (U3-5 HIGH)
- Phase 1 clocks running
- MODE flag from Mode Condition Generator.

The design of the PN generator for the Sounder and the Prober modes are basically the same, differing only in the details relating to the length of the PN sequence. The basic components are a shift register(s) with the appropriate feedback connections to generate the desired sequence, a magnitude comparator(s) for generating the reference pulse, and suitable logic

for gating the appropriate sequence according to the designated operating mode. A description of the operation of the Sounder Mode PN generator, Figure 4, will suffice to explain that of the Prober Mode generator as well.

The basic input to the PN sequence Generator is the 31.25 kHz clock which is connected to the PN sequence shift register at U27-8 (Figure 4). The pulse out of U41-15 is fed to the input of the shift register at U27-1 to set up an initial condition of all 1's in the shift register at START TIME. Thereafter, the shift register operates continuously with the PN sequence appearing at U27-13 and fed to the output line driver at U23-6 (8T13). The magnitude comparators (U31, U32) compare the instantaneous state of the shift register with a reference state set up by a series of switches. A comparator match produces a coincidence output pulse at U32-6 which is used as a μP interrupt. This pulse is gated through U34, U37, and a Schmitt trigger line driver at U22. The gating signal is derived from the experiment START/STOP signal (from U3-5) as conditioned by flip-flops at U36.

The line driver at U23 (8T13) is common to the Sounder and Prober mode PN generators. Using the START/STOP signal line and the Sounder/Prober mode "ON" signal, the appropriate sequence is gated to the BPSK modulator of the Transmitter Exciter. It should be noted that both the Sounder mode and the Prober mode interrupts are continuously passed to the μP regardless of operating mode. The μP selects the appropriate signal according to the prevailing operating mode.

D. Mode Condition Generator

The Mode Condition Generator alters the action of the Timing Module according to the operating mode as prescribed by the Control Module. Inputs to the Mode Condition Generator include:

- MODE flag from the μP
- MODE initialization pulse from the START/STOP circuit
- Phase-1 and phase-2 clock signals.

Mode Condition Generator outputs include:

- Appropriately selected phase-2 clock for distribution to the Transmitter Exciter
- Sounder mode and Prober mode ON/OFF flags for distribution to the PN Generator circuits
- Sounder mode Prober mode ON/OFF indicator lamps.

During normal operation, the MODE flag from the microprocessor serves to toggle the state of the Mode Condition Generator. Manual override is provided via switches S3 and S4 (refer to Figure 6) which permit manual setting of the operational mode for circuit test purposes.

A circuit diagram of the Mode Condition Generator is shown in Figure 6. The generator can be analyzed in terms of a Sounder section and a Prober section where the action is essentially the same in both.

U17 comprises a pair of flip-flops designed so that U17-5 is LOW when U17-9 is HIGH and vice versa. This condition enables one mode or the other, but not both. In a quiescent state the preset (PR) and clear (CLR) pins of both flip-flops are HIGH and the output state is stable (e.g., U17-9 LOW, U17-5 HIGH, Prober Mode). Simultaneous negative transitions at U17-10 (Sounder set) and at U17-1 (Prober reset), resulting from activation of the single-shot multivibrator at U14-12, reverses the output state of U17 (i.e., U17-9 HIGH, U17-5 LOW) and thereby reverses the mode of operation from Prober mode to Sounder mode. In a similar fashion, a negative pulse at U14-4 will toggle the U17 flip-flops back to the Prober Mode condition.

A negative going pulse at U14-12 can be produced in several ways. During continuous operation, mode toggling results from a transition of the MODFLG signal level at U22-3. Transition from a LOW (Prober Mode) to a HIGH (Sounder Mode) will activate the single-shot multivibrator at U14-12. Similarly the transition from a HIGH (Sounder) to a LOW (Prober) activates the single-shot output at U14-4 and these actions toggle the mode condition flag, U17.

A second action which will affect the operating mode is the manual closure of mode switch S3 or S4. Closure of either switch will activate the single-shot multivibrators at U14.

Finally, the initialization signals at U16-2 and U16-12 clear flip-flops U12 and U13 and then excite the Sounder Mode by activation of the single-shot multivibrator at U15-12. This, in turn, leads to the activation of U14-12 and a HIGH at U17-9, thus insuring Sounder Mode at START TIME.

The Timing Module is mounted on a PC board which plugs into the μP "mother" board. A photograph of the Timing Module board showing the locations of numbered integrated circuit chips is presented in Figure 7. The control switches, indicator lamps and various interconnection cable connectors are mounted on a separate panel. Figure 8 is a photograph of that panel.

E. 8 MHz Phase Locked Loop

The 8 MHz clock is generated for the Correlation Processor coherent clock. Although considered part of the Timing Module, the circuit is not physically located on the Timing Module circuit board. The circuit diagram for the 8 MHz clocks is shown in Figure 9 and consists of four integrated circuit chips, U1 to U4, and transistor Q1.

The circuit is driven by the system 1 MHz reference oscillator. The 1 MHz sine wave is transformed to a square wave by the action of Q1. The square wave is the input to a 4046 CMOS phase-locked loop (U1) that operates

at 1 MHz. The dc voltage output of U1 is the input to a 74LS124 voltage controlled oscillator (U4) that operates at 16 MHz. The 16 MHz output of U4 is the clock input to a 74161 binary counter (U3). The divide by 16 (1 MHz) output of U3 controls the phase-locked loop. The output of U3 at 8 MHz (divide by 2 output) is the input to a 8T13 line driver (U2). The output of U2 is a symmetric square wave at 8 MHz that is conditioned to a 50 ohm line.

IV. Microprocessor Control Module

A. Microprocessor Hardware

The microprocessor selected uses a Motorola 6802 MPU chip and is part of the Model 9600A/ Option 1, single board microprocessor manufactured by Creative Microsystems Inc. Included on the 9600A board are the following features:

- 128 bytes of on-chip (Model 6802) RAM
- 1K byte of RAM with battery back-up
- 6K bytes of EPROM
- 2, ACIA serial interfaces (Model 6850)
- 2, PIA parallel interfaces (Model 6821)
- 1, Programmable Timer Module (Model 6840)

In addition, the system is supported by a second "plug-in" board providing 32K of static RAM.

The primary means of experiment control is achieved with the parallel interface adapter chips (PIA). Each PIA provides sixteen individually controllable signal lines, each individually configured by software as either input or output. In addition, each PIA has four more signal lines, two of which are strictly input lines used for interrupts, while the remaining two are input/output lines used either for interrupt or "handshaking" purposes.

The asynchronous communications interface adapter chips (ACIA) are basically communication drivers and serve to convert serial data to parallel and vice versa. The 9600A board provides drivers to implement either, RS-232 or 20 ma current loop, communication protocol. One serial interface is dedicated to service the control console, which in this case is a Texas Instruments Model 733 ASR, Silent-700 terminal. The other communications interface is dedicated to communication with the DEC Model PDP-11/34 minicomputer either locally or via telephone circuits

Only one section of the Programmable Timer Module (PTM) is used and its function is to produce a delayed pulse for the computer controlled AGC. The PTM is designed to operate in a single-shot pulsed mode when an experiment is in progress. The single-shot pulse is always timed to occur during

sequence 1 (the "idle" sequence) of a correlation cycle* and is delayed a few milli-seconds relative to the start of the sequence to allow for system settling time. Receiver gain is held constant at the value determined by the computer controlled AGC until sequence 1 of the next correlation cycle.

A diagram of μP memory organization is given in Figure 10. The 6K bytes of EPROM are located in the top of the memory which contains 65K bytes of addressable memory. The top 2K bytes of EPROM are reserved for the system Monitor which is a manufacturer-provided operating system for software development. The next lower 2K bytes of EPROM are dedicated to user developed system utilities such as a cassette tape handler, etc. The lower 2K bytes of EPROM are dedicated to the user operating program. In the current application the Control Module operating system starts at hexadecimal address E800 and ends at EF99 which is almost the entire 2K byte EPROM.

The 32K bytes of RAM are configured to occupy the lowest 32K bytes of memory and are used mainly to accommodate the large programs required for software development.

B. Microprocessor Software

Specific tasks to be performed by the Control Module include:

- Control experiment mode
- Control signal frequency
- Control Receiver pre-selector filter and input attenuator (Receiver site only)
- Indirect control, via MODE flag, of gating of the clock and PN generator output to the Transmitter Exciter (Transmitter site only)
- Control gating of the Receiver computer controlled AGC function (Receiver site only)
- Control experiment duration

The block diagram in Figure 1 summarizes the interaction between the Control Module and the other major components of the system.

The μP software can be broken up into two major subdivisions, the Control Executive and the Interrupt Handler. The Control Executive is responsible for general housekeeping, communication, and initialization activities while the Interrupt Handler is responsible for updating the state of the experiment and controlling experiment variables according to the PN sequence count.

---

*The interested reader is referred to Wagner, Goldstein, and Chapman, 1982 for details relating to overall system operation.

1. Control Executive

A flow diagram of the Control Executive is shown in Figure 11. Major subdivisions of the Control Executive are Communication and Initialization functions which are identified in Figure 11. In addition, the Run Loop and End of Run Housekeeping functions are designated in Figure 11. The Run Loop of the Control Executive is the area of μP software where execution awaits interrupts from the Timing Module.

The communications and initialization functions are completed prior to experiment start. Experiment start awaits the arrival of the first interrupt from the Timing Module. Once the experiment has started, the Control Executive executes the short loop while awaiting further interrupts. The only activity during this loop is a check for change of mode and a check of the STOP flag. Upon detection of a STOP flag, the program executes the End of Run Housekeeping functions and returns to the start of the communication routine where it waits for the next experiment parameter message from the PDP-11/34. The Programmable Timer Module (PTM) is initialized to a continuous mode of operation during the communication portion of the μP software. The purpose of the continuous mode is to implement AGC action prior to experiment start. The PTM is switched to the single-shot mode of operation after receipt of the first interrupt from the Timing Module.

The communication software represents approximately one half the code required for the Control Executive. It is responsible for communicating with the PDP-11/34 either locally or via telephone circuits using Motorola serial tape format. The purpose of the communication is to provide the Control Module with the data needed to perform the experiment. The routine provides for automatic error checking at several levels as well as a final operator approval or disapproval after reviewing the message. Error correction is accomplished by automatic block repetition in the case of routine errors and by repetition of the entire message if the operator believes the data to be suspect. The communication protocol calls for short blocks (16 data bytes) and automatic block repetition if a positive block acknowledgment is not received. Figure 12 is a flow diagram of the communication function. The input data, along with some descriptive commentary, are summarized in Table I.

Error free data are stored in μP RAM according to the allocation shown in Figure 13. Memory is organized into 256 byte groups called pages. The first 8 pages of RAM (pages 0 to 7) are allocated to experiment data storage. Pages 4 through 6 are used for frequency tables for the Sounder mode and page 7 is used for Prober frequency tables. In these tables, the 10^7, 10^6 and 10^5 Hertz digits of the frequency are represented in BCD format. Page zero is dedicated to the storage of experiment constants, count variables, pointers and flags. A detailed organization of the page zero memory is given in Figure 14. Page 1 of RAM memory is dedicated to the User Program Stack while pages 2 and 3 are presently not used.

Experiment parameters, as received from the PDP-11/34, are printed on the microprocessor control console. An example of this printout is given in Figure 15. Frequencies are printed out in decimal notation in units of 10^4 Hz. All other experiment parameters are printed in hexadecimal notation. Upon examination of this printout, the operator decides whether to continue with the experiment or whether to request a repeat of the transmission from the PDP-11/34.

2. Interrupt Handler

The interrupt handler routine is responsible for orchestrating the functions of the other HF Channel Prober System Modules. It keeps track of the current sequence number and signals the minicomputer at the appropriate time to start a new correlation cycle. It also implements changes in frequency and mode as prescribed by the experiment format and signals all other system modules when the experiment is over.

The Interrupt Handler tasks may be summarized as follows:

- Set up all flags, counters, and frequency BCD signals at the start of a correlation cycle.
- Strobe the receiver AGC Sample gate during PN sequence 1, after an appropriate settling-time delay.
- Signal the Correlation Processor to START during PN sequence 2.
- Keep count of the number of completed correlation cycles, modifying experiment mode and frequency scanning action according to the prescribed format.
- Terminate the experiment after the prescribed number of repetitions of the Sounder mode.

The Timing Module sends an interrupt reference signal to the Control Module at the start of each Sounder and Prober mode PN sequence. Only one or the other interrupt is recognized by the Control Module depending upon the current mode of the experiment. Receipt of an interrupt causes the μP to interrupt the Run Loop (Figure 11) in the Control Executive and to proceed to the Interrupt Handler routine where all control variables are updated according to the prescribed experiment format. A summary of the μP output variables along with details of format, function and destination is given in Table II.

The action of the Interrupt Handler software is described in the flow diagram of Figure 16. Notice that the Interrupt Handler can recognize the first interrupt of an experiment and uses that knowledge to re-initialize the PTM of the Control Module to the single-shot mode of operation.

The Control Module interacts with the other system modules such as the Receiver, Transmitter Exciter, Timing Module and Real-Time Processor (PDP-11/34) via the PIA. The μP comes equipped with two PIAs (PIA #1, PIA #2), each of which has 16 individually controllable I/O lines (A0-A7, B0-B7) and four additional lines (CA1, CA2, CB1, CB2) used for interrupt and hand-shaking purposes. Table III shows the distribution of the PIA-I/O lines, which support the control functions shown in Figure 1. It should be noted that CB1 on both PIA's is used as an interrupt input line. CB2 on PIA#1 is used as a frequency latching line, a requirement of the system local oscillator. All lines are individually software controllable and it is the function of the Interrupt Handler to ensure their proper setting. The DR11C is the PDP-11/34 parallel interface board used for transferring control signals between the Control Module and the Real-Time Processor.

V. SUMMARY AND CONCLUSION

The hardware and software implementation of the timing and control functions for the Wideband HF Channel Prober project have been presented. Design considerations have been stated and discussed. The operation of the resulting hardware has been explained and the overall functioning of the control software has been presented. The interaction between the Timing and Control Modules and other system modules are detailed.

The actual operation of the Timing Module has shown that it performs the various system functions as designed and in a reliable fashion. The Control Module has also performed well and its flexibility has been exploited through software improvements that field operations have dictated.

In conclusion, the Timing and Control Module satisfies system requirements and results in smooth data collection for the Wideband HF Channel Prober.

VI. REFERENCE

1. Wagner, Goldstein and Chapman, 1982, "Wideband HF Channel Prober-System Description, NRL Report 8622.

TABLE I - Microprocessor Input Data

VARIABLE NAME	ARRAY SIZE	FUNCTIONAL DESCRIPTION
NUMXFR(I*)	2	Max # correlation cycles/mode
FFMAX(I*)	2	Max # of fixed frequency correlation cycles/mode
INTEG'N(I*)	2	# of PN sequences to be integrated
FMX(I*)	2	# of frequencies per scan cycle
FFSNDR	1	Sounder mode fixed frequency index
TBLSNDR(J)	N	Array of Sounder frequencies (XX.X MHz, BCD); up to 255 frequencies
FFPRBR	1	Prober mode fixed frequency index
TBLPRBR(J)	M	Array of Prober frequencies (XX.X MHz, BCD); up to 30 frequencies

*Where I = 1, Prober Mode
I = 2, Sounder Mode

TABLE II - Microprocessor Outputs

VARIABLE NAME	DESTINATION	VARIABLE FORMAT	# PINS	FUNCTION
FRQD7	L.O. Receiver/ Transmitter Exciter	BCD	3	Remote control 10^7 Hz digit of frequency synthesizer.
FRQD6	L.O. Receiver/ Transmitter Exciter	BCD	4	Remote control 10^6 Hz digit of frequency synthesizer.
FRQD5	L.O. Receiver/ Transmitter Exciter	BCD	4	Remote control 10^5 Hz digit of frequency synthesizer.
SLCTD7	Receiver Pre-Selector	BCD	2	Remote control 10^7 Hz digit of Receiver Preselector.
SLCTD6	Receiver Pre-Selector	BCD	4	Remote control 10^6 Hz digit of Receiver Preselector.
AGCGATE	Receiver AGC	1 Bit	1	2×10^{-3} sec TTL voltage pulse for AGC strobe.
FPTR	PDP-11/34 Real-Time Processor	Binary	8	Frequency index, identifies current operating frequency.
MODFLG	PDP-11/34/ Timing Module	1 Bit	1	Serves as a mode ID and also as a gating signal to the Transmitter Exciter.
IDSQFG	PDP-11/34 Real-Time Processor	1 Bit	1	Identifies 1st and 2nd PN sequences in a frequency correlation cycle.
IDS2FG	PDP-11/34 Real-Time Processor	1 Bit	1	Identifies 2nd PN sequence in a correlation cycle. Enables start of Correlation Processor.
STPFLG	PDP-11/34 & Timing Module	1 Bit	1	Flag signaling experiment stop.
FLTCH	L.O. Receiver/ Transmitter Exciter	1 Bit	1	0.6×10^{-6} sec TTL voltage pulse for latching synthesizer remote frequency lines.

Table III - MICROPROCESSOR I/O - PERIPHERAL CONNECTIONS

Peripheral Side Terminal or Pin #			Microprocessor Side Interface Pin #
			PIA#1, A0
	10^6 Hz digit,		PIA#1, A1
	(BCD)		PIA#1, A2
			PIA#1, A3
Receiver/	10^6 Hz digit,		PIA#1, A4
Transmitter	(BCD)		PIA#1, A5
Local Oscillator			PIA#1, A6
Frequency			PIA#1, A7
	10^7 Hz digit		PIA#1, B0
	(BCD)		PIA#1, B1
			PIA#1, B2
TIMING MODULE		(MODFLG)	PIA#1, B4
PDP 11/34	DR11C, D12	(MODFLG)	PIA#1, B5
	DR11C, D13	(STPFLG)	PIA#1, B6
TIMING MODULE		(STPFLG)	PIA#1, B7
	DR11C, D0		PIA#2, A0
	DR11C, D1		PIA#2, A1
	DR11C, D2		PIA#2, A2
PDP 11/34	DR11C, D3	(FPNTR)	PIA#2, A3
	DR11C, D4		PIA#2, A4
	DR11C, D5		PIA#2, A5
	DR11C, D6		PIA#2, A6
	DR11C, D7		PIA#2, A7
PDP 11/34	DR11C, D14	(IDLS2 FLG)	PIA#2, B0
	DR11C, D15	(IDSQ FLG)	PIA#2, B1
	10^6 Hz Digit		PIA#2, B2
Receiver	(BCD)		PIA#2, B3
Pre-Selector			PIA#2, B4
			PIA#2, B5
	10^7 Hz Digit		PIA#2, B6
	(BCD)		PIA#2, B7
TIMING PROBER	Reference Pulse	(Interrupt)	PIA#1,CB1
MODULE SOUNDER	Reference Pulse	(Interrupt)	PIA#2,CB1
Receiver/Transmitter	Local Osillator	(FLTCH)	PIA#1,CB2
Receiver		AGC STROBE	TIMER#3,O3

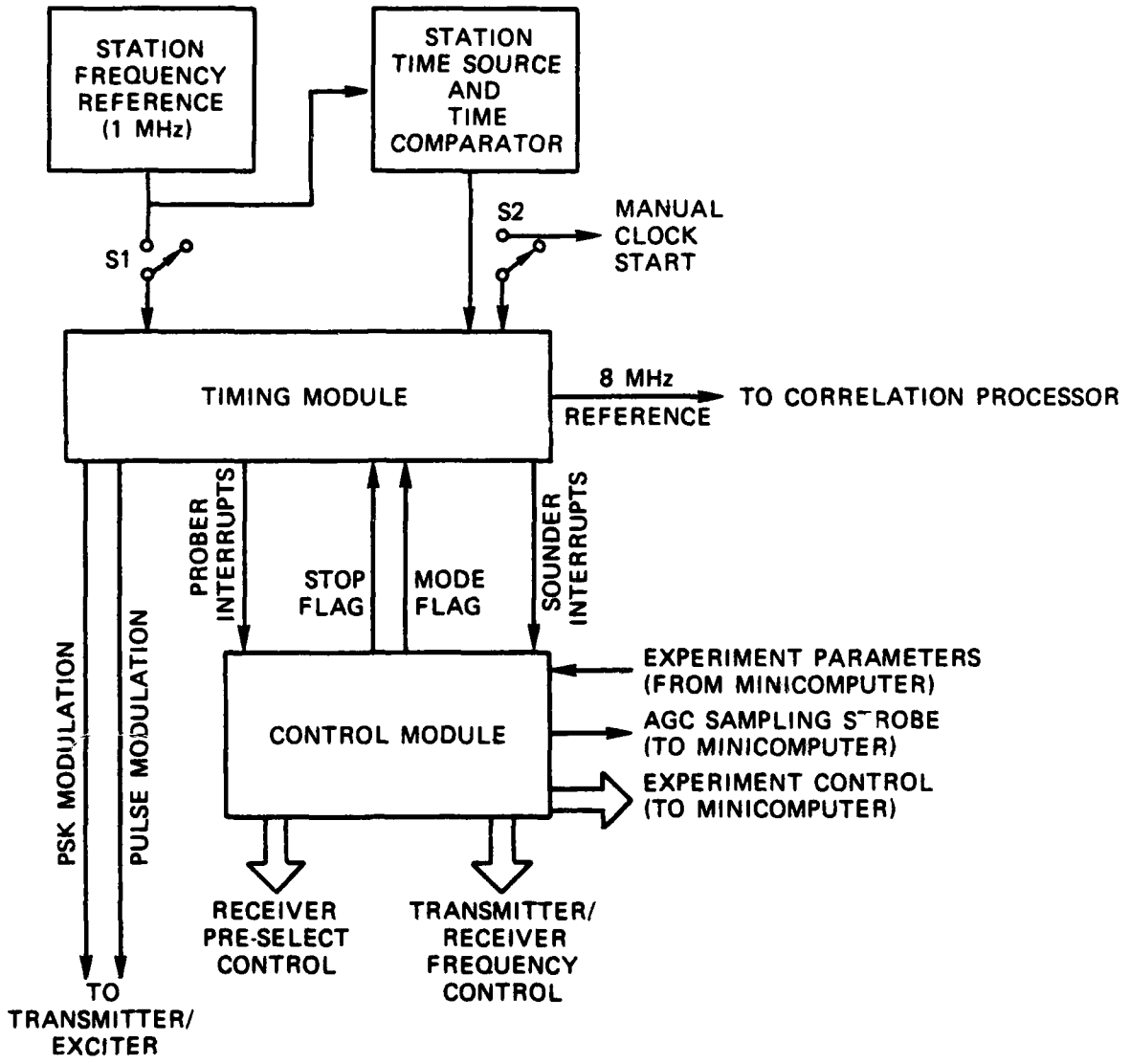


Fig. 1 — Block diagram of Timing and Control Modules

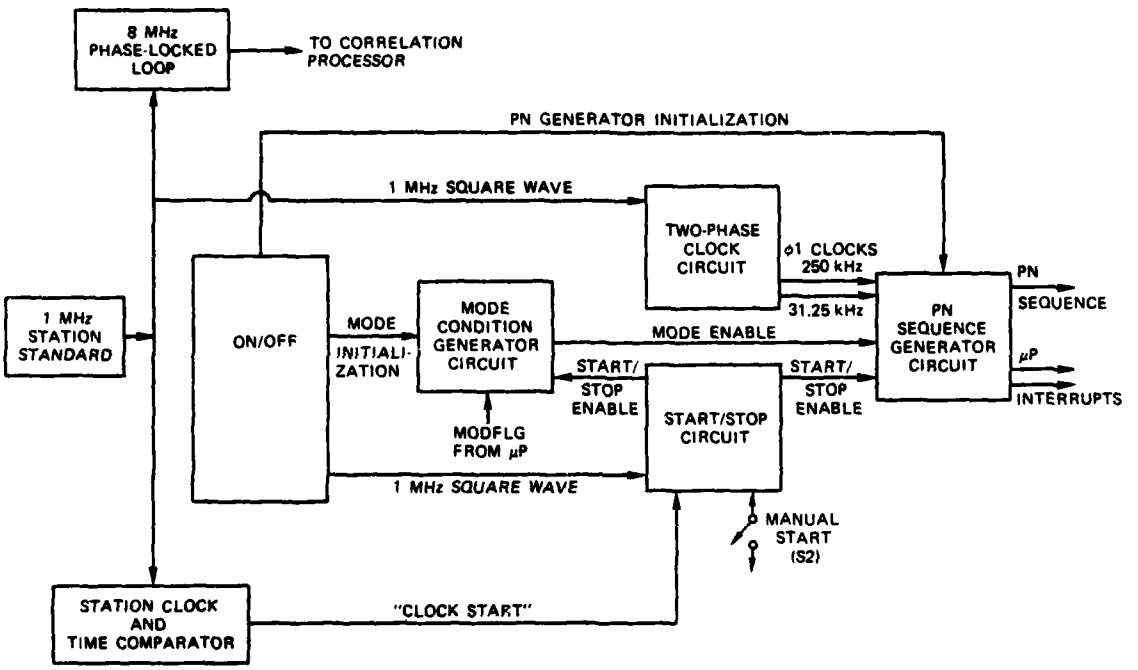


Fig. 2 — Block diagram of the Timing Module

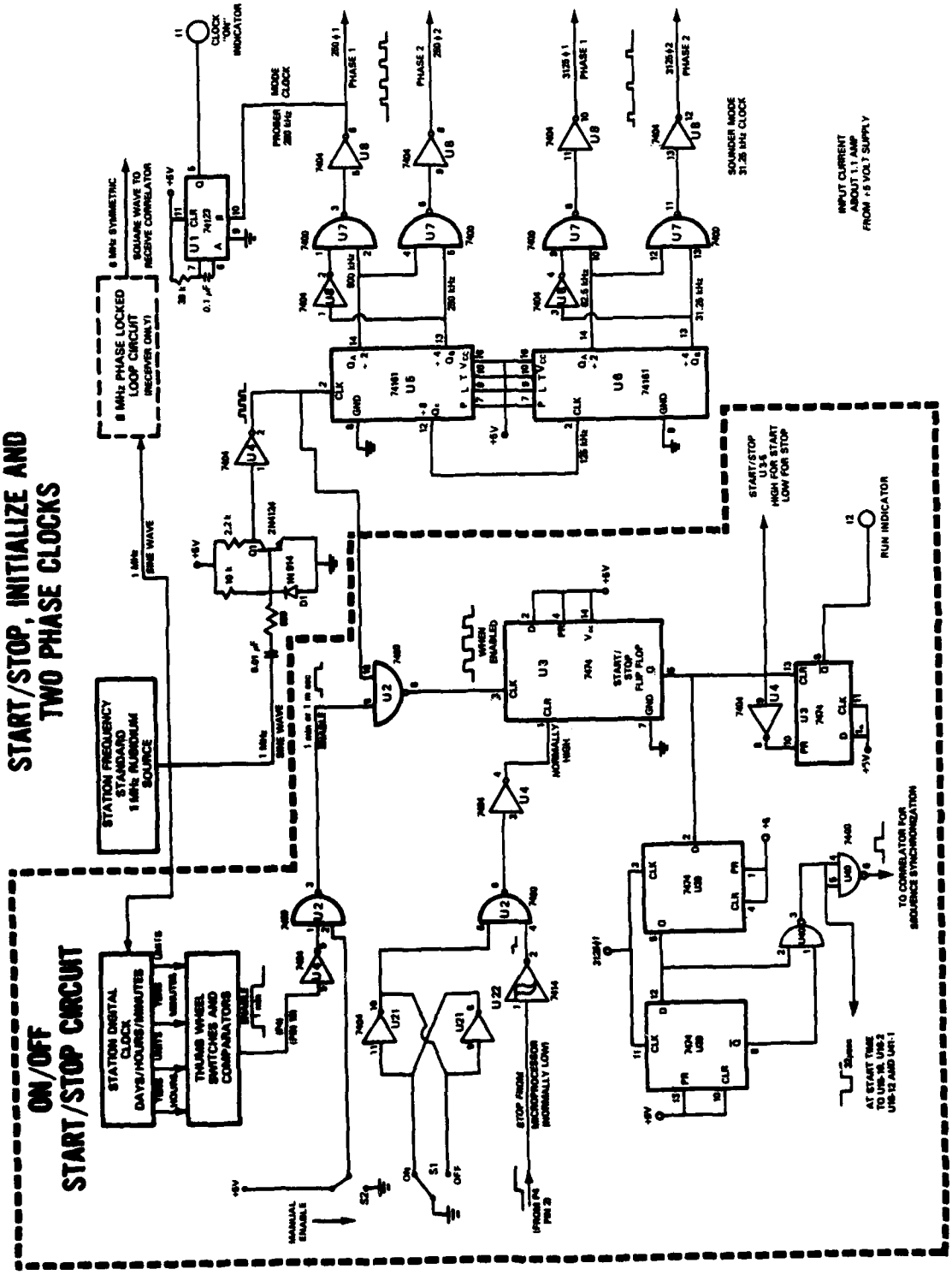


Fig. 3(a) — ON/OFF and START/STOP logic circuits

START/STOP, INITIALIZE AND TWO PHASE CLOCKS

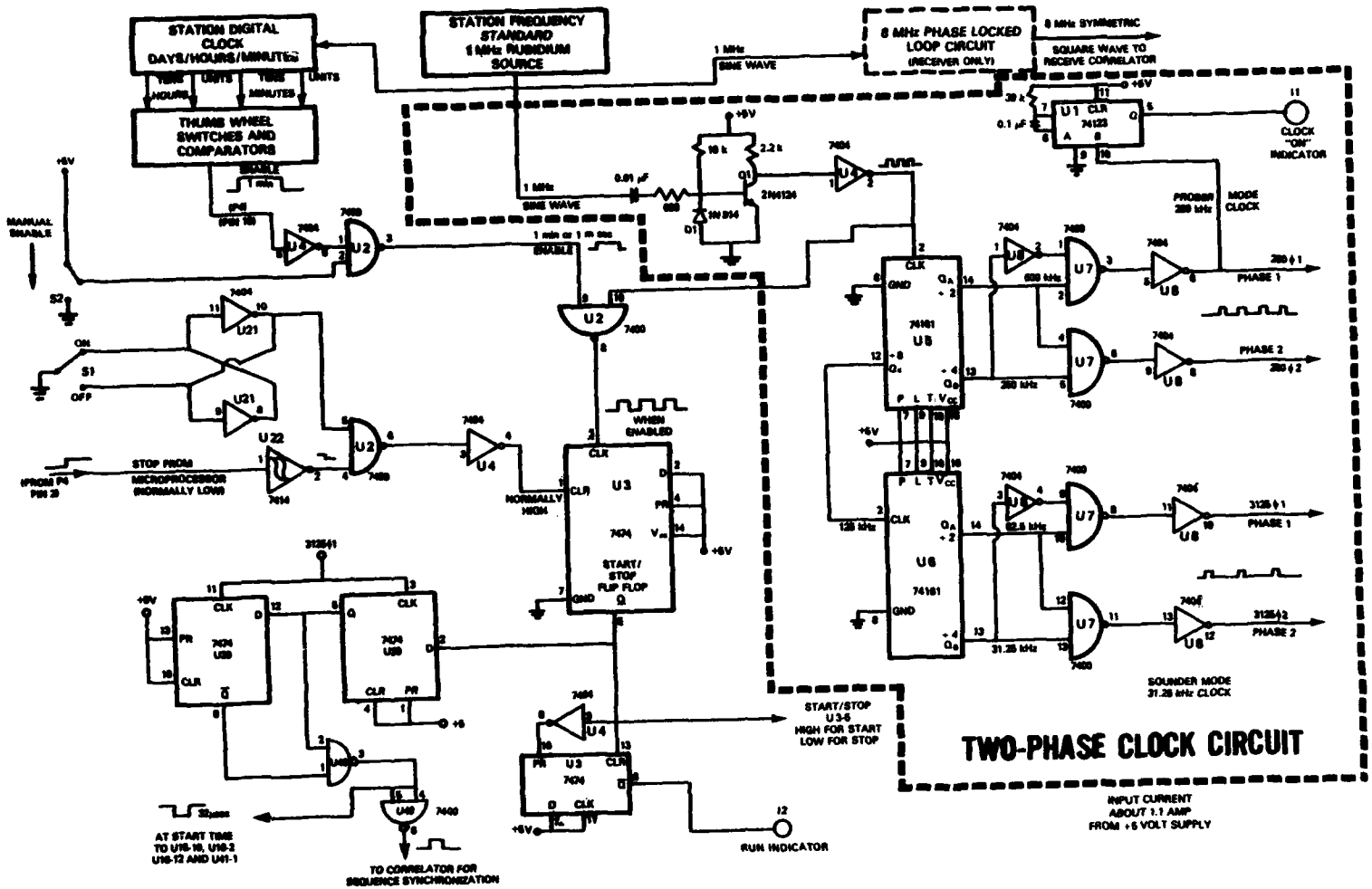


Fig. 3(b) — Two-Phase Clock logic circuit

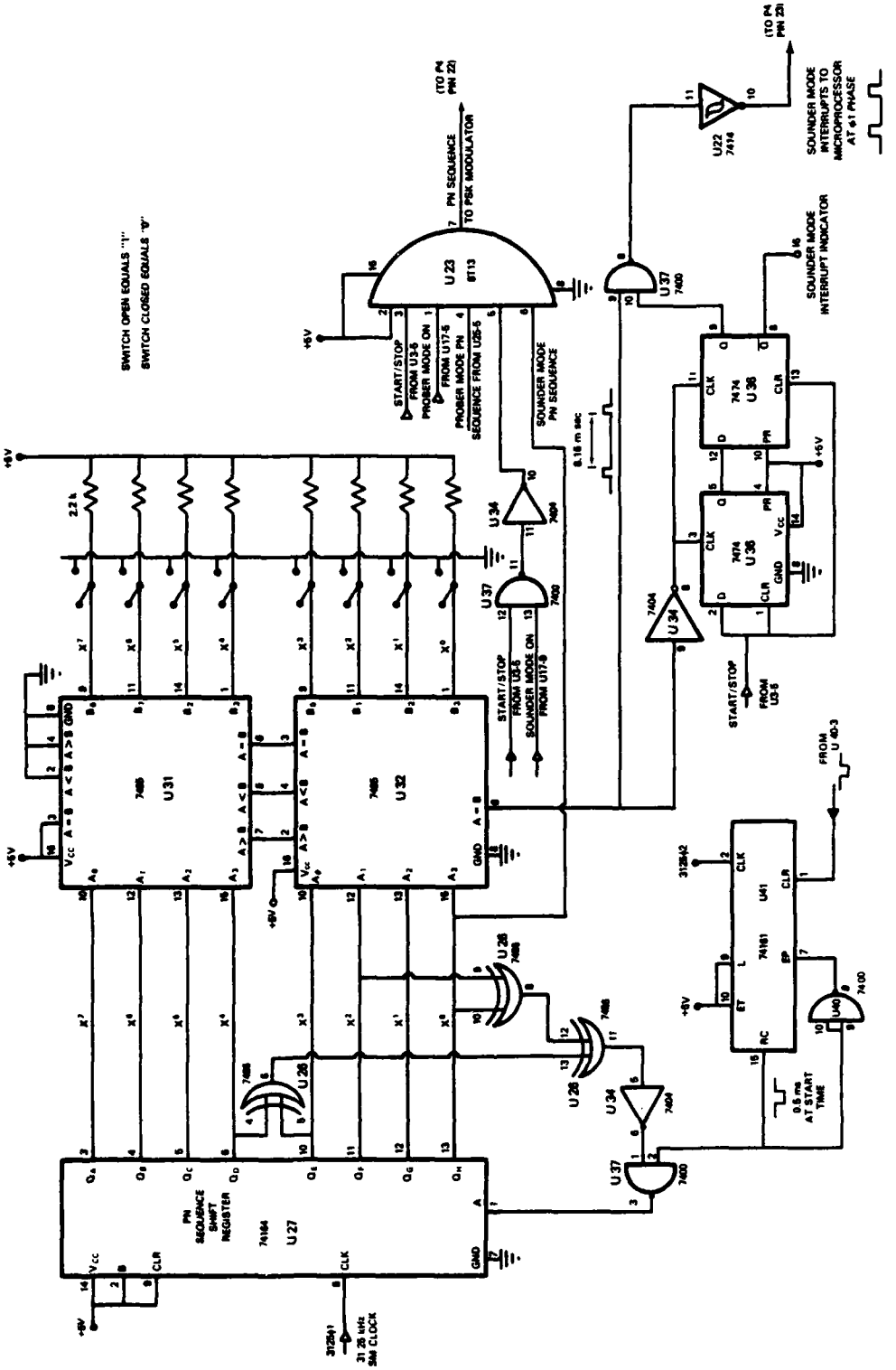


Fig. 4 — Sounder Mode PN Sequence Generator logic circuit

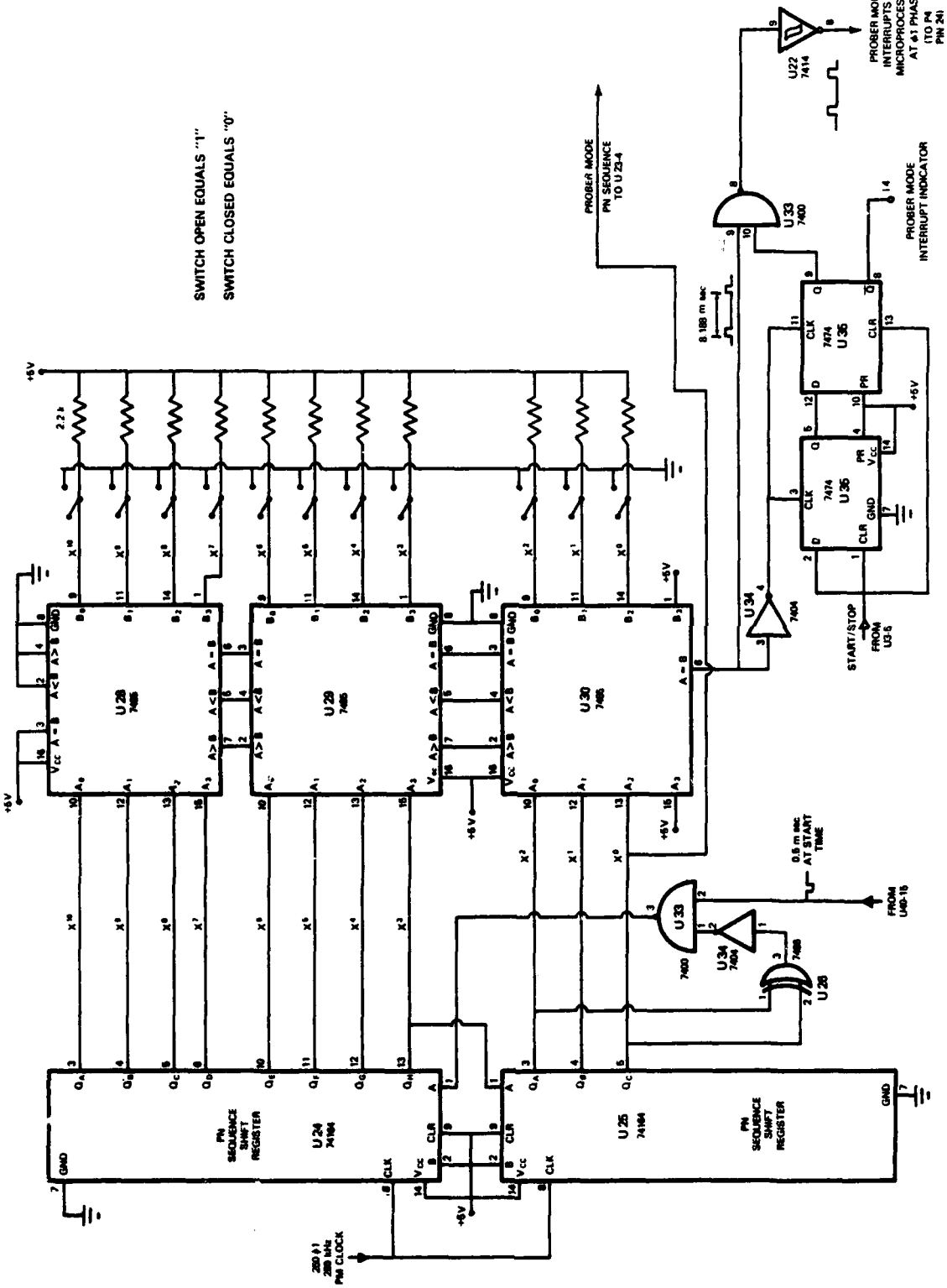


Fig. 5 — Prober Mode PN Sequence Generator logic circuit

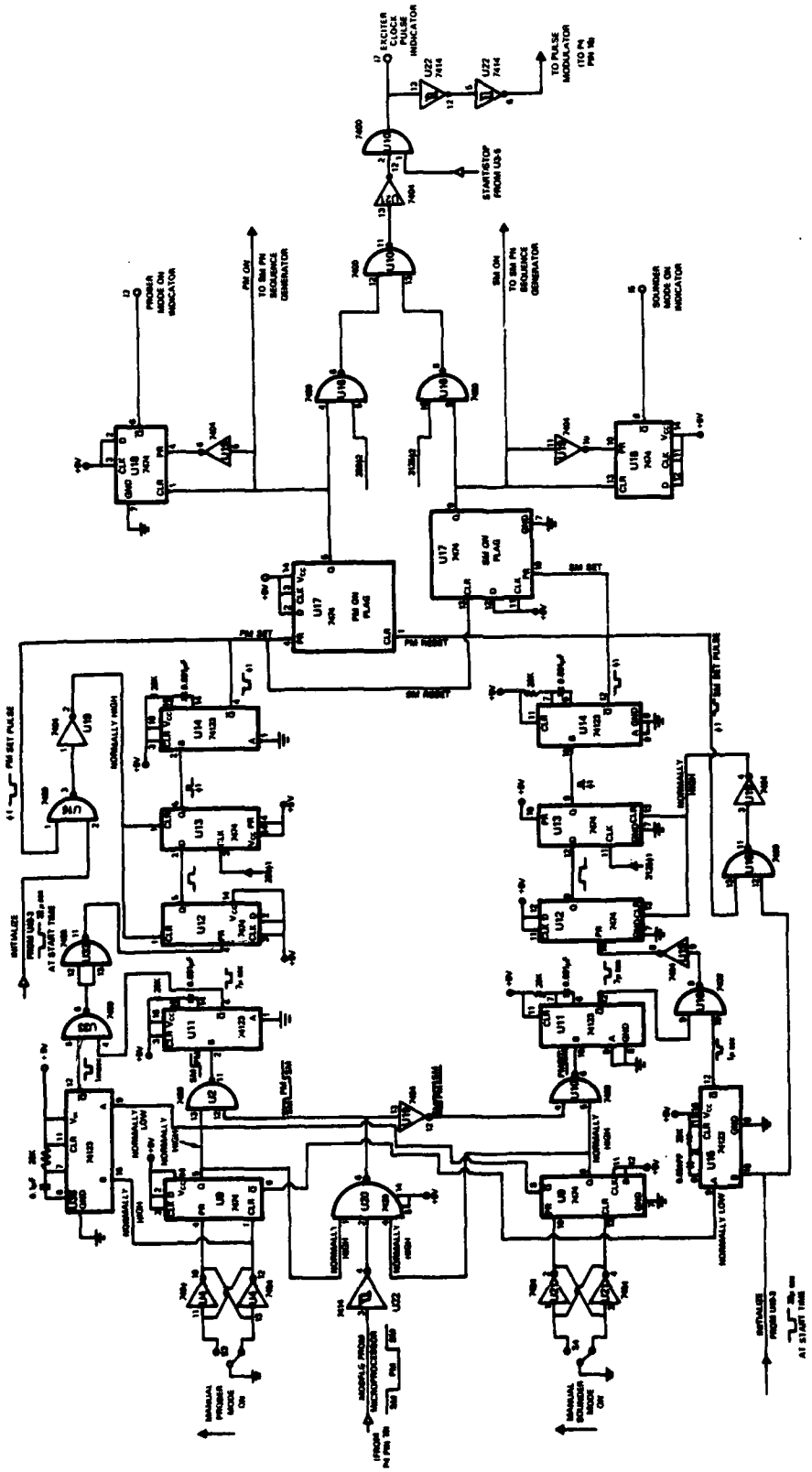


Fig. 6 – Mode Condition Generator logic circuit

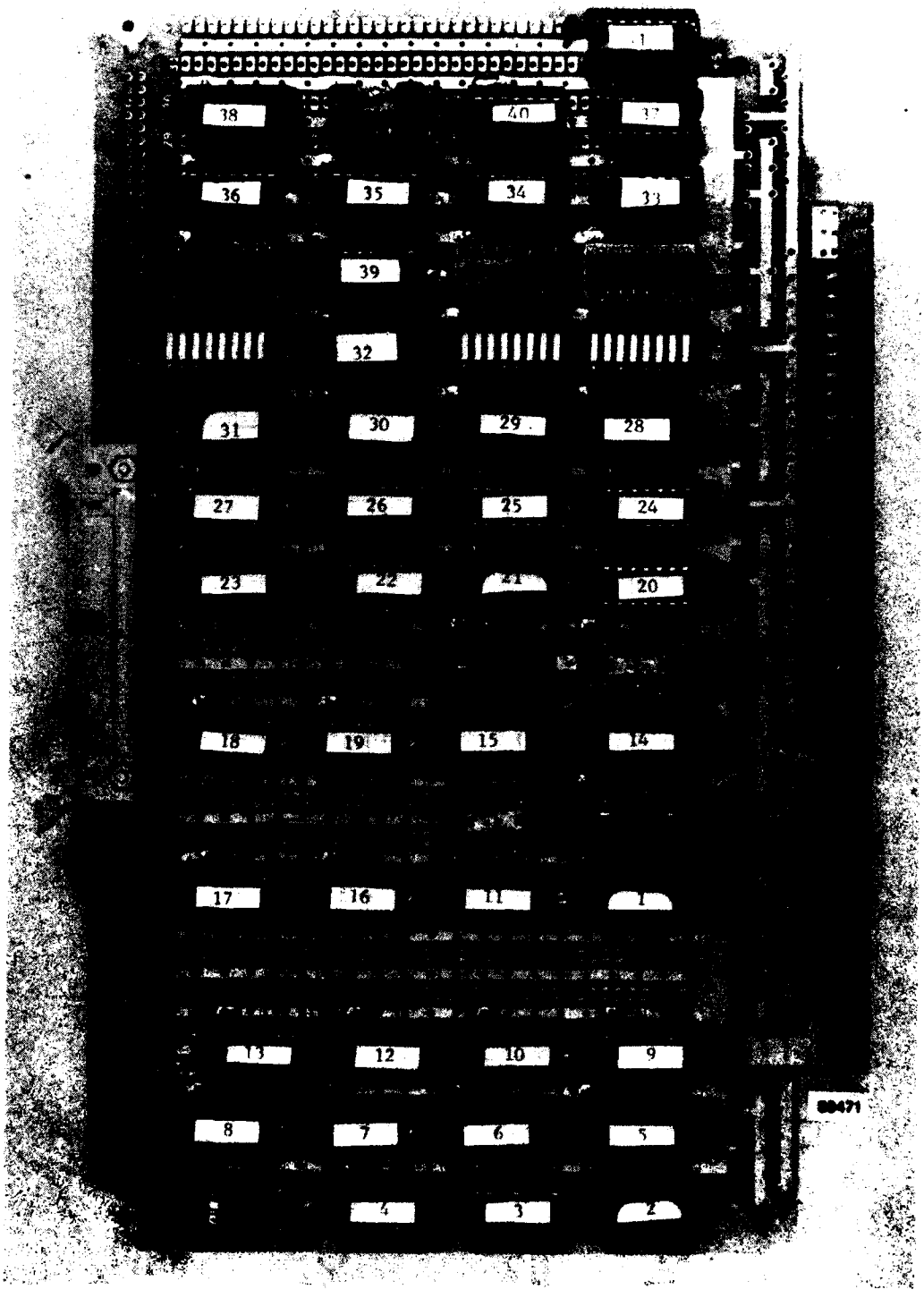


Fig. 7 — Timing Module circuit component layout

Fig. 8 — Timing Module panel illustrating the switches, indicator lamps and interconnection cable connectors

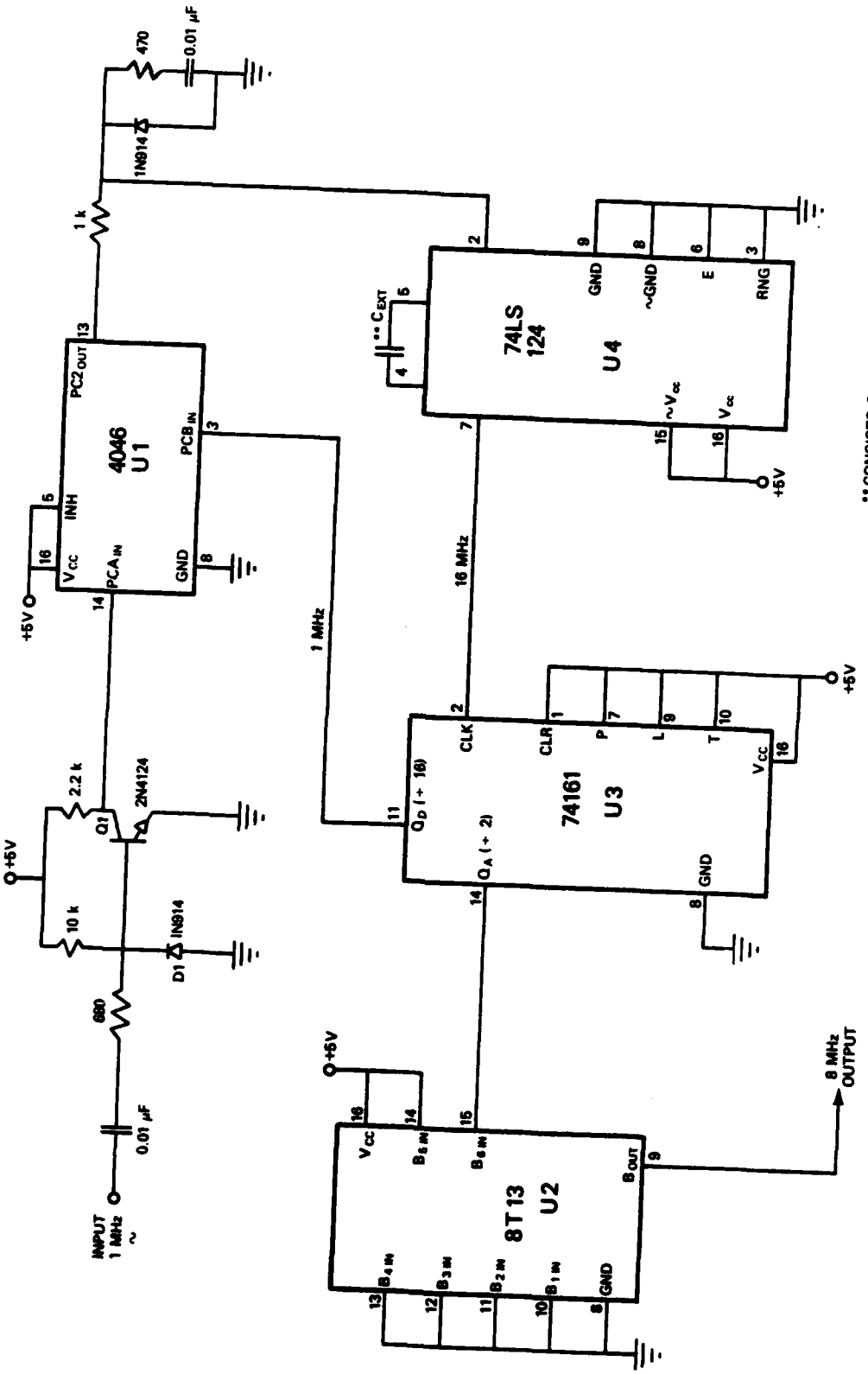


Fig. 9 — 8 MHz Square Wave Generator logic circuit

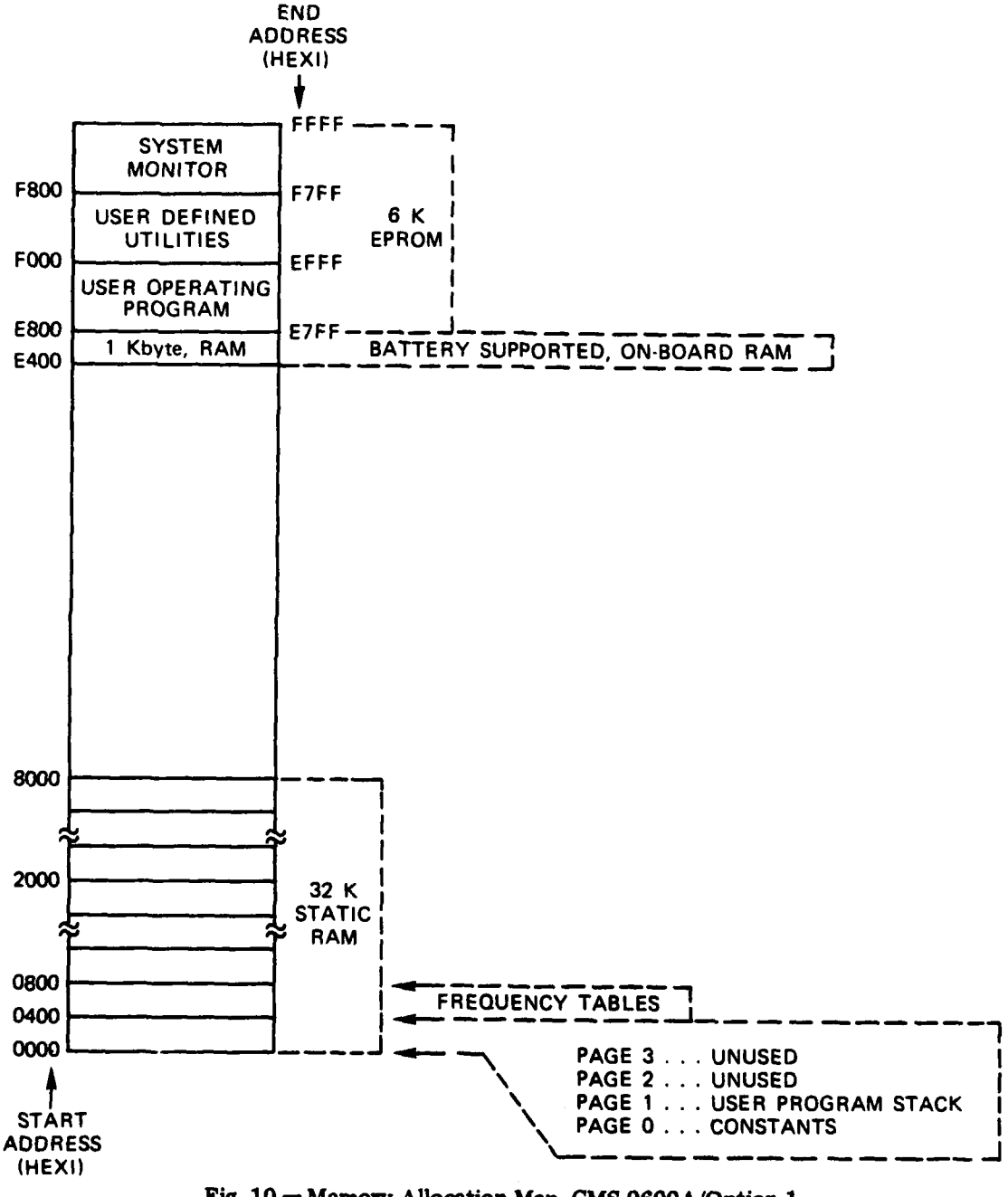


Fig. 10 — Memory Allocation Map, CMS 9600A/Option 1

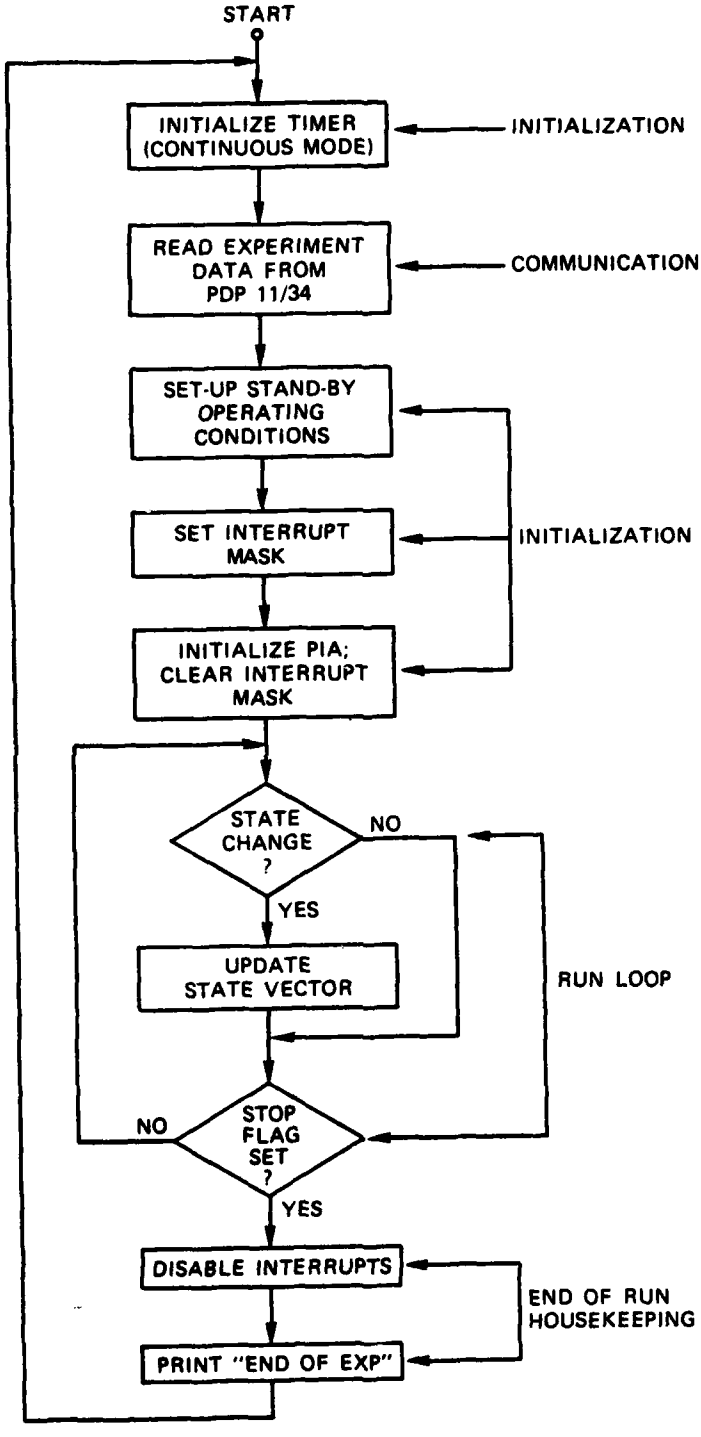


Fig. 11 — μP Control Executive flow diagram

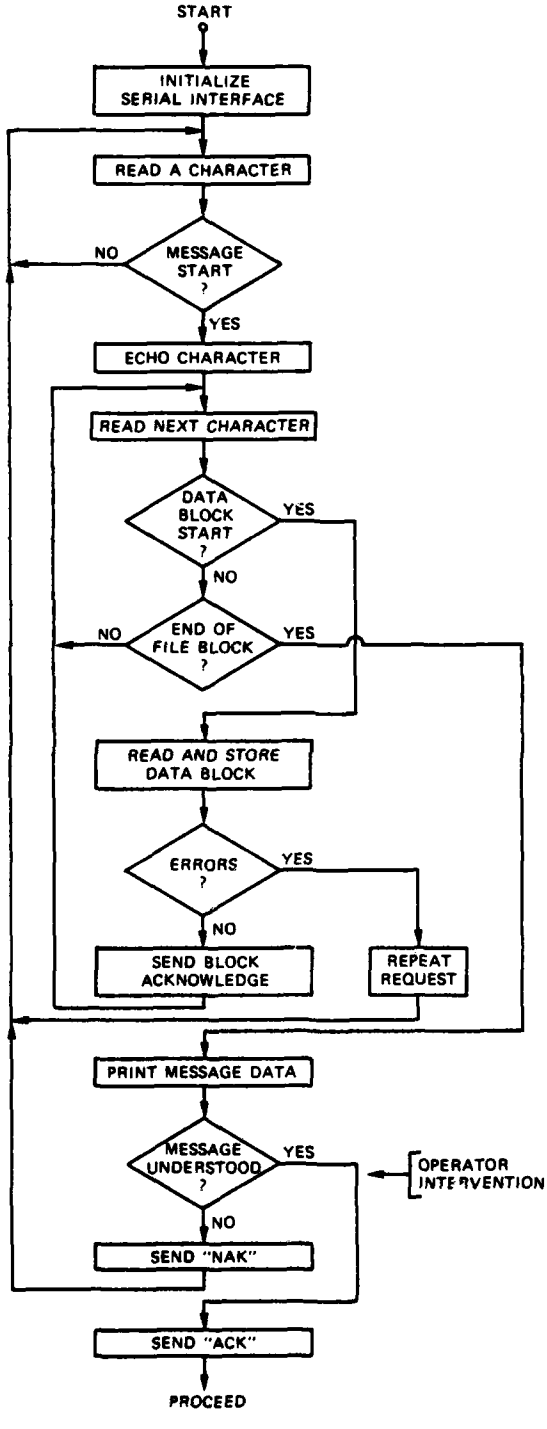


Fig. 12 — μP Communication Software flow diagram

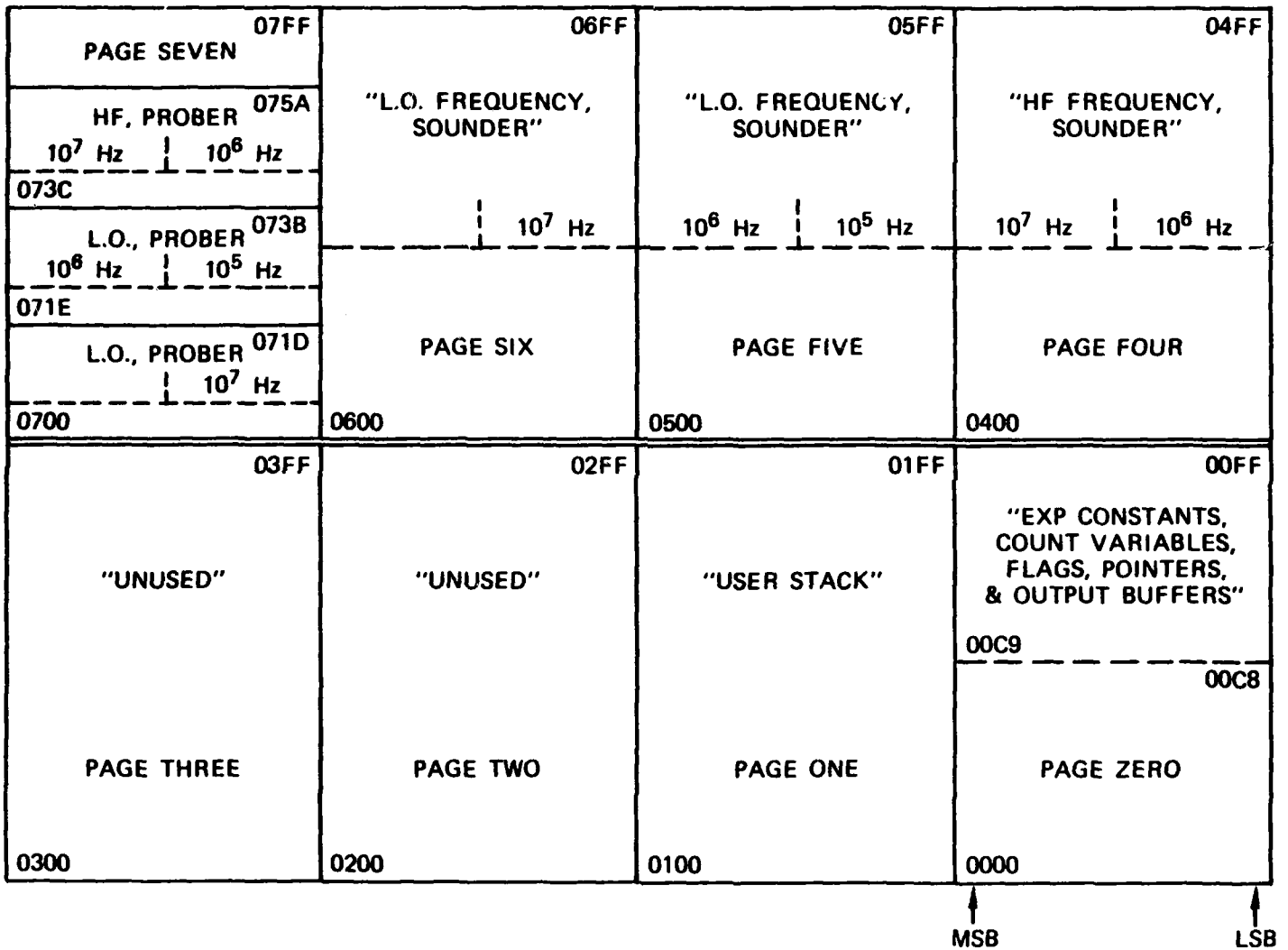


Fig. 13 — μP RAM Allocation, pages 0 to 7

	00FF	FFPR	
	00FE	FMXPRB	
	00FD	RPMX	PROBER
	00FC	FFMX (L)	MODE
	00FB	FFMX (H)	CONSTANTS
	00FA	NUMXFR (L)	
	00F9	NUMXFR (H)	
	00F8	FFSR	
	00F7	FMXSND	
	00F6	RPMX	SOUNDER
	00F5	FFMX (L)	MODE
	00F4	FFMX (H)	CONSTANTS
	00F3	NUMXFR (L)	
	00F2	NUMXFR (H)	
	00F1	STPMX/STPCNT	STOP COUNTER
	00F0	FFPT	
	00EF	FMX	OPERATING
	00EE	RPCT	CONSTANTS
	00ED	FFCT (L)	&
	00EC	FFCT (H)	COUNT
	00EB	SCCT (L)	VARIABLES
	00EA	SCCT (H)	
	00E9	PA1	PIA
	00E8	PB1	OUTPUT
	00E7	PA2	VARIABLES
	00E6	PB2	
	00E5	SVC2	STATE
	00E4	SVC1	VECTORS
	00E3	IDS2	SEQUENCE
	00E2	IDSQ	FLAGS
	00E1	XHI (L)	
	00E0	XHI (H)	SCRATCH PAD
	00DF	TMP1 (L)	
	00DE	TMP1 (H)	
	00DD	BAS3 (L)	
	00DC	BAS3 (H)	
	00DB	BAS2 (L)	FREQUENCY TABLE
	00DA	BAS2 (H)	BASE ADDRESSES
	00D9	BAS1 (L)	
	00D8	BAS1 (H)	
	00D7	PRFG	PRELIM FLAG
	00D6	RPMX	NO. SEQUENCES/CORR'N CYCLE
	00D5	TMP2 (L)	SCRATCH PAD
	00D4	TMP2 (H)	
	00D3	CMFG	COMMUNICATIONS FLAG
HEXI ADDRESS →	00C9	MPFG	MODE POSITIONING FLAG

BIT CONFIGURATION

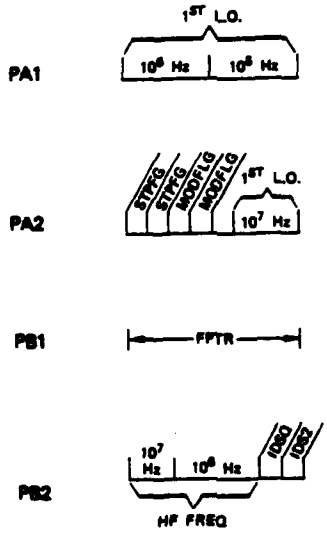


Fig. 14 — μP Page Zero Storage Allocation

SOUNDER FREQ TABLE

1110	1120	1130	1140	1150	1160	1170	1180	1190	1200	1210	1220	1230	1240	1250
1260	1270	1280	1290	1300	1310	1320	1330	1340	1350	1360	1370	1380	1390	1400
1410	1420	1430	1440	1450	1460	1470	1480	1490	1500	1510	1520	1530	1540	1550
1560	1570	1580	1590	1600	1610	1620	1630	1640	1650	1660	1670	1680	1690	1700
1710	1720	1730	1740											

PROBER FREQ TABLE

1110	1210	1310	1410	1510	1610	1710	1810	1910	2010

EXP CONSTS	SOUNDER	PROBER
TOTAL CORR'NS/MODE	0048	0026
NO. OF FF CORR'NS/MODE	0008	0008
NO. SEQ/CORR'N	41	41
NO. OF FREQS	40	0A
FF POINTR	02	03

NO. MODE CYCLES 02

Fig. 15 — Example of Experimental Parameters Printout on the μP Terminal

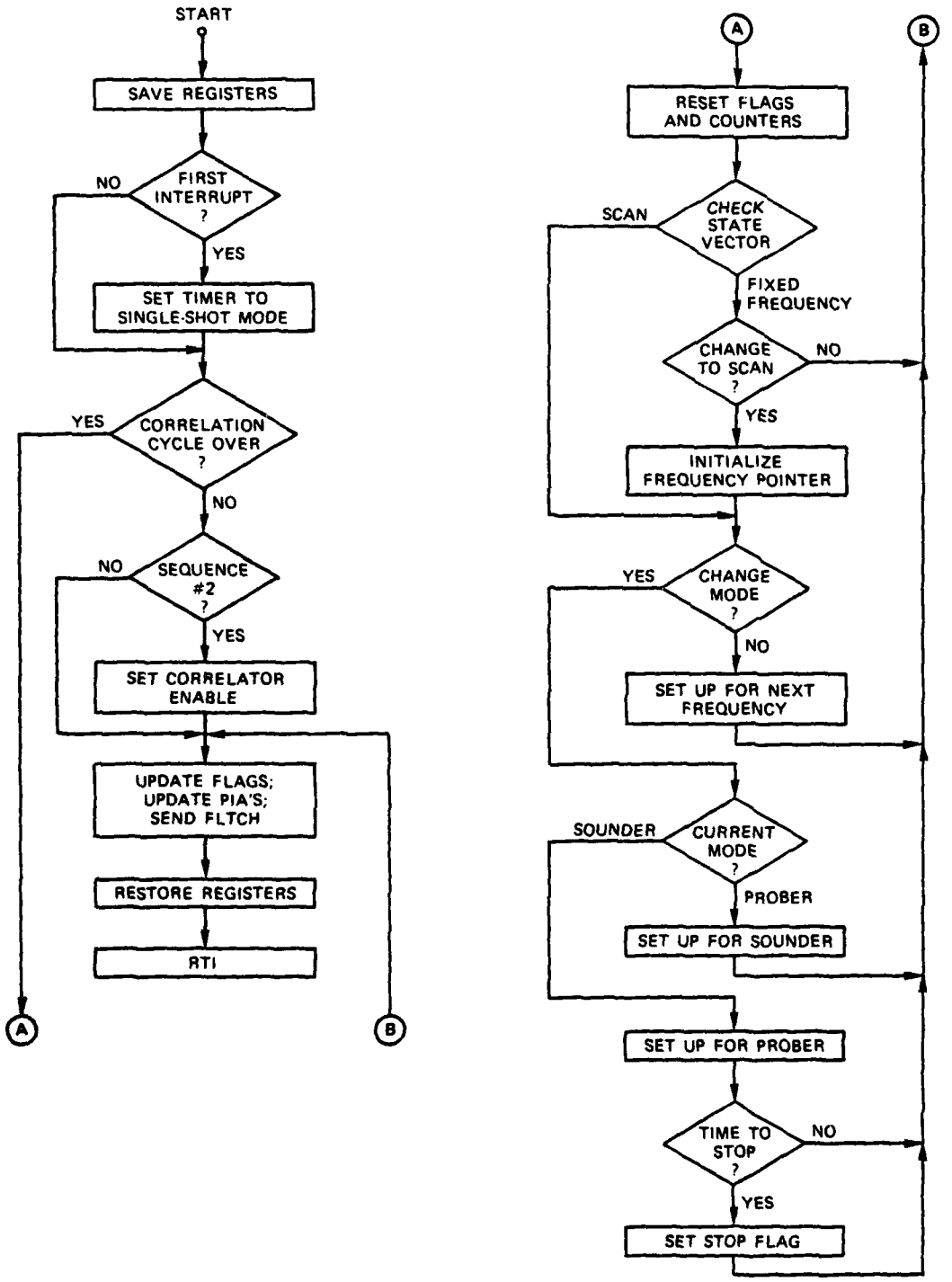
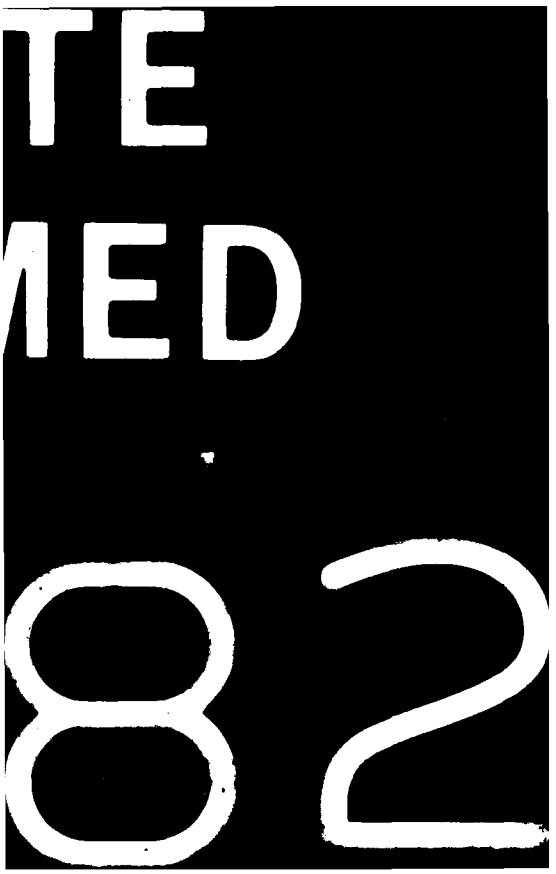


Fig. 16 — Interrupt Handler flow diagram


TE
MED
82